WHAT IS CLAIMED IS:

1. A microprocessor comprising an instruction processor, an instruction decoder to decode the output from said instruction processor, and a processor to make calculations according to the output from said instruction decoder, wherein when the instructions that are input are specified instructions said instruction processor outputs said input instructions to said instruction decoder, and when the input instructions are other than said specified instructions, a first instruction different from said input instructions is output to said instruction decoder.

2. A microprocessor according to claim 1, wherein said instruction processor has an instruction discriminator circuit and an instruction selector circuit, and said discriminator circuit determines whether or not the instruction input into said instruction processor is said specified instruction, and based on said discrimination results, said instruction selector circuit selects either said first instruction or said input instruction and outputs either said first instruction or said input instruction to said instruction decoder.

3. A microprocessor according to claim 1 or claim 2, wherein said specified instruction is an instruction to perform calculations in said processor.

4. A microprocessor according to claim 1 ~~through~~ claim 3, wherein said first instruction is an NOP instruction.

5. A microprocessor according to claim 1 ~~through~~ claim 3, wherein said first instruction is an instruction for a designated code.

6. A microprocessor according to claim 1 ~~through~~ claim 5, wherein said processor is a processor for a designated processing circuit.

7. A microprocessor according to claim 6, wherein said designated processor is a floating point unit.

8. A microprocessor according to claim 1 ~~through~~ claim 7, wherein said processor calculates the data stored in a first latch and outputs said calculated results to a second latch, and the supply of clock pulses to said first latch and said second latch is halted when said first instruction is input to said instruction decoder.

9. A microprocessor according to claim 1 ~~through~~ claim 8, further comprising a second register to receive instructions, a second instruction decoder connected to said second register, and a second processor controlled by the output of said second instruction decoder, wherein the instruction supplied to said instruction processor circuit and the instruction input to said second register are the same instruction.

10. A microprocessor according to claim 1 ~~through~~ claim 9, wherein said microprocessor is formed on the same semiconductor substrate.

11. A microprocessor comprising an instruction processor circuit input with instructions, an instruction register to receive the output of said instruction processor circuit, an instruction decoder to decode the output of said instruction register, and a processor to perform calculations according to decoded results from said instruction decoder, wherein said instruction processor circuit halts the supply of clock pulses to said instruction register when the instructions that were input are other than the specified instructions.

12. A microprocessor according to claim 11, comprising an instruction discriminator circuit, and a control circuit to supply clock pulses to said instruction register, wherein said instruction discriminator circuit determines whether or not the instruction input to said instruction processor circuit is said specified instruction and outputs said discrimination results to said control circuit, said control circuit, based on said discrimination results, stops the supply of clock pulse to said instruction register when an instruction other than the specified instruction was input.

13. A microprocessor according to claim 11, comprising an instruction discriminator means and a control means, wherein said instruction discriminator means determines whether or not the instruction input to said instruction processor circuit is said specified instruction and outputs said discrimination results to said control means, and said control means based on said discrimination results, stops the supply of clock pulse to said instruction register when an instruction other than the specified instruction was input.

14. A microprocessor according to claim 11 ~~through~~ claim 13, wherein said specified instruction is an instruction to perform calculations in said processor.

15. A microprocessor according to claim 11 ~~through~~ claim 14, wherein said processor is a processor for a designated processing circuit.

16. A microprocessor according to claim 11 ~~through~~ claim 15, wherein said processor performs calculations of data stored in a first latch and outputs said calculated data to a second latch, and the supply of clock pulses for said first latch and said second latch is stopped when an instruction other than the specified instruction was input to said instruction processor circuit.

17. A microprocessor according to claim 11 ~~through~~ claim 16, further comprising a second register to receive instructions, a second instruction decoder connected to said second register, and a second processor controlled by the output of said second instruction decoder, wherein the instruction supplied to said instruction processor circuit is the same as the instruction input to said second register.

18. A microprocessor according to claim 11 ~~through~~ claim 17, wherein said microprocessor is formed on the same semiconductor substrate.

19. A microprocessor comprising an instruction processor circuit, an instruction decoder to decode the output of said instruction processor circuit, and a processor to make calculations according to decoding results from said decoder, wherein when the instruction that is input is other than the specified instruction, said instruction processor circuit does not supply to said instruction decoder the instruction that is input.

20. A microprocessor according to claim 19, comprising an instruction processor circuit, an instruction discriminator circuit and switching circuit, wherein said instruction discriminator circuit determines whether or not the instruction input to said instruction processor circuit is said specified instruction and outputs said discrimination results to said switching circuit, and based on said discrimination results, opens the electrical connection between said discriminator circuit and said instruction decoder when an instruction other than the specified instruction was input.

21. A microprocessor according to claim 19 or claim 20, wherein said specified instruction is an instruction to perform calculations in said processor.

22. A microprocessor according to claim 19 ~~through~~ claim 21, wherein said processor is a processor for a designated processing circuit.

23. A microprocessor according to claim 22, wherein said designated processor is a floating point unit.

24. A microprocessor according to claim 19 ~~through~~ claim 23, wherein said processor performs calculations of data stored in a first latch and outputs said calculated data to a second latch, and the supply of clock pulses for said first latch and said second latch is stopped when an instruction other than the specified instruction was input to said instruction processor circuit.

25. A microprocessor according to claim 19 ~~through~~ claim 24, further comprising a second register to receive instructions, a second instruction decoder connected to said second register, and a second processor controlled by the output of said second instruction decoder, wherein the instruction supplied to said instruction

processor circuit is the same as the instruction input to said second register.

26. A microprocessor according to claim 19 ~~through~~ claim 25, wherein said microprocessor is formed on the same semiconductor substrate.

27. A microprocessor comprising an instruction processor circuit input with instructions from the memory, a first decoder to decode the output of said instruction processor circuit, a first processor to make calculations according to decoding results from said first decoder, a second decoder to decode the output from said instruction processor circuit, and a second processor to calculate the output according to decoding results from said second decoder, wherein when the instruction that is input is not the instruction to perform calculations in said second processor, the power consumption by said second decoder is reduced versus the power consumption of said first decoder.

28. A microprocessor according to claim 27, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculations in said second processor, an instruction is

output for said second decoder that is different from the instruction that is input.

29. A microprocessor according to claim 28, wherein said different instruction is an NOP instruction.

30. A microprocessor according to claim 27, comprising an instruction register between said second decoder and said instruction processor circuit, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculations in said second processor, said instruction processor circuit stops the supply of clock pulses to said instruction register.

31. A microprocessor according to claim 27, comprising a switching circuit between said second decoder and said instruction processor circuit, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculations in said second processor, said instruction processor circuit controls said switching circuit, and opens the connection between said instruction processor circuit and said second decoder.

32. A microprocessor comprising an instruction processor circuit, a first decoder to decode the output of said instruction processor circuit, a first processor to make calculations according to the decoding results from said first decoder, a second decoder to decode the output from said instruction processor circuit, and a second processor to make a calculation according to decoding results from said second decoder, wherein when the instruction that is input is not the instruction to perform calculations in said second processor, an instruction is output for said second decoder that is different from the instruction that is input.

33. A microprocessor according to claim 32, wherein said different instruction is an NOP instruction.

34. A microprocessor according to claim 32 or claim 33, wherein said first processor is an arithmetic logic unit, and said second processor is a processor with a designated calculator circuit.

35. A microprocessor according to claim 34, wherein said designated calculator circuit is an FPU.

36. A microprocessor according to claim 32 through 35, wherein said second processor calculates the data stored in the first latch, and outputs the calculation results to the second latch and,

when the instruction input to said instruction processor circuit is not the instruction to perform calculation in said second processor, said instruction processor circuit stops the supply of clock pulses to said first latch and to said second latch.

37. A microprocessor according to claim 32 through 36, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculation in said first processor, said instruction processor circuit does not output said input instruction to said first decoder.

38. A microprocessor according to claim 32 through 37, wherein said microprocessor is formed on the same semiconductor substrate.

39. A microprocessor comprising an instruction processor circuit, a first decoder to decode the output of said instruction processor circuit, a first processor to make calculations according to decoding results from said

first decoder, a second decoder to decode the output from said instruction processor circuit, and a second processor to make a calculation according to decoding results from said second decoder, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculations in said second processor, said instruction processor circuit does not output said input instruction to said second decoder.

40. A microprocessor according to claim 39, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculations in said second processor, said instruction processor circuit supplies an instruction different from the input instruction, to said second decoder.

41. A microprocessor according to claim 39, further comprising an instruction register with said second decoder input by the output of said instruction processor circuit, said instruction processor circuit further has a control circuit, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculations in said second processor, said control circuit stops the supply of clock pulses to said instruction register.

42. A microprocessor according to claim 39, further comprising a switching circuit with said second decoder input by the output of said instruction processor circuit, said instruction processor circuit further has a control circuit wherein, when the instruction input to said instruction processor circuit is not the instruction to perform calculations in said second processor, said instruction processor circuit controls the switching circuit, opening the connection between said instruction processor circuit and said second decoder.

43. A microprocessor according to claim 39 through claim 42, wherein said first processor is an arithmetic logic unit, and said second processor is a processor with a designated calculator circuit.

44. A microprocessor according to claim 43, wherein said designated calculator circuit is an FPU.

45. A microprocessor according to claim 39 through 42, wherein said second processor calculates the data stored in the first latch, outputs the calculation results to the second latch, and when the instruction input to said instruction processor circuit is not the instruction

to perform calculation in said second processor, the supply of clock pulses is stopped to said first latch and to said second latch.

46. A microprocessor according to claim 39 through 45, wherein when the instruction input to said instruction processor circuit is not the instruction to perform calculation in said first processor, said instruction processor circuit does not output said input instruction to said first decoder.

47. A microprocessor according to claim 39 through 46, wherein said microprocessor is formed on the same semiconductor substrate.

48. A microprocessor comprising an instruction processor means, a first decoder means to decode the output of said instruction processor means, a processor to make calculations according to decoding results from said first decoder means, wherein when the instruction input to said instruction processor means is other the specified instruction, said instruction processor means does not output said input instruction to said first decoder.

49. A microprocessor according to claim 48, wherein said specified instruction is an instruction for performing calculations in the processor for the designated calculator circuit.

50. A microprocessor according to claim 48 or 49, wherein said processor calculates the data stored in a first latch and outputs the calculation results to a second latch, and when the instruction input to said instruction processor means is other than said specified instruction, the supply of clock pulses to said first latch and said second latch is stopped.

51. A microprocessor according to claim 48 through claim 50, further comprising a second register to receive instructions, a second decoder means connected to said second register, and a second processor controlled by the output of said second decoder means, wherein the instruction supplied to said instruction processor circuit is the same as the instruction input to said second register.

52. A microprocessor comprising an instruction processor circuit input with instructions, a instruction decoder input with the output of said instruction processor

circuit, and a processor to make calculations according to decoding results from said instruction decoder, wherein

said instruction processor circuit has a selector circuit to select either a first instruction different from the input instruction or said input instruction, and a discriminator circuit input with a specified bit of said input instruction, and wherein

when said specified bit is a first status, said discriminator circuit controls said selector circuit and outputs said first instruction to said instruction decoder, and

when said specified bit is not a first status, said discriminator circuit controls said selector circuit to output said input instruction to said instruction decoder.

53. A microprocessor comprising an instruction processor circuit input with instructions, a instruction decoder input with the output of said instruction processor circuit, and a processor to make calculations according to decoding results from said instruction decoder,

said instruction processor circuit has a selector circuit to select either a first instruction different from the input instruction or said input instruction, and a control register, wherein

when said specified bit of said control register is a first status, said selector circuit is controlled to output said first instruction to said instruction decoder, and

when said specified bit of said control register is not a first status, said selector circuit is controlled to output said input instruction to said instruction decoder.

54. A microprocessor according to claim 52 or claim 53, wherein said first instruction is an NOP instruction.

55. A microprocessor according to claim 52 or claim 53, wherein said first instruction is a designated code.

56. A microprocessor according to claim 52 through claim 55, wherein said processor is the processor of a designated calculation circuit.

57. A microprocessor comprising an instruction processor circuit input with instructions, a instruction decoder input with the output of said instruction processor

circuit, and a processor to make calculations according to decoding results from said instruction decoder,

said instruction processor circuit has a discriminator circuit input with the specified bit of said input instruction, and a control circuit to receive the output of said discriminator circuit, wherein

when said specified bit is a first status, said discriminator circuit controls said control circuit to stop the operation of said first decoder.

58. A microprocessor comprising a clock control circuit, an instruction processor circuit input with instructions, an information register input with the output of said instruction processor circuit, an instruction decoder input with the output of said instruction register, and a processor circuit to make calculations according to decoding results from said instruction decoder,

said instruction processor circuit has a discriminator circuit input with the specified bit of said input instruction, and has a switching circuit to receive the output of said discriminator circuit connected to said instruction register and to the output of said clock control circuit, wherein

when said specified bit is a first status, said instruction processor circuit controls said switching

circuit to stop the supply of clock pulses to said instruction register.

59. A microprocessor comprising an instruction processor circuit input with instructions, a switching circuit input with the output of said instruction processor circuit, a instruction decoder input with the output of said switching circuit, and a processor to make calculations according to decoding results from said instruction decoder,

said instruction processor circuit has a discriminator circuit input with the specified bit of said input instruction, wherein

when said specified bit is a first status, said instruction processor circuit controls said switching circuit to open the connection between said instruction processor circuit and said instruction decoder.

60. A microprocessor according to claim 57 through claim 59, wherein said processor is the processor of a designated calculation circuit.

61. Portable electronic equipment installed with the microprocessor of claim 19 ~~through~~ claim ~~28~~ 20.

wherein said portable electronic equipment is capable of operating on battery power.

62. Portable electronic equipment installed with the microprocessor of claim 39 through claim 42, wherein said portable electronic equipment is capable of operating on battery power.